IN THE CLAIMS

Claims 15-23 are pending in this application.

1-14. (Canceled)

15. (Previously Presented) A semiconductor integrated circuit, comprising:

an address conversion memory circuit for converting a logical address of a vertical memory into a physical address of a main memory,

wherein the address conversion memory circuit comprises a gated logic circuit, a clock enable generating circuit, a tag memory and a data memory,

wherein clocks are supplied to the tag memory and the data memory via the gated logic supplies and cuts off the clocks,

wherein the tag memory stores the logical page address as tag information,

wherein the data memory stores the physical page address as entry information,

wherein the clock enable generating circuit invalidates a clock enable signal when a first logical page address requested as a preceding access is the same as a second logical page address requested as a present access and a first intra-page address requested as the present access is not within the boundary addresses between intra-page addresses, and

wherein the gated logic circuit cuts off the clock to the tag memory and the data memory when the clock enable signal is valid.

16. (Previously Presented) A semiconductor integrated circuit according to claim 15,

wherein the address conversion memory circuit further comprises a status register which stores a valid bit indicating whether or not to use the virtual memory, and

wherein the clock enable generating circuit invalidates the clock enable signal when the valid bit being invalid.

17. (Previously Presented) A semiconductor integrated circuit according to claim 15, further comprising:

an instruction cache for reading instructions; and

a data cache for reading and writing data,

wherein the clock enable generating circuit invalidates the clock enable signal when the clock enable generating circuit receives a cache stall-signal indicating that cache-miss occurs in the instruction cache and the data cache.

18. (Previously Presented) A semiconductor integrated circuit, comprising:

a processor executing compressed instructions of VLIW instruction in which a plurality of instruction codes are arranged in a plurality of fields,

wherein the compressed instructions comprise effective instruction codes except codes of NOP instructions and instruction location information indicating locations of the plurality of instruction codes,

wherein the processor comprises an instruction cache, an instruction unit, an instruction decoder, an execution unit and a plurality of gated clock circuits,

wherein the instruction unit comprises an instruction location information decoder,

wherein the instruction decoder comprises a plurality of decode circuits in order to simultaneously decode the plurality of instruction codes,

wherein the execution unit comprises a plurality of execution circuits to simultaneously process in parallel the plurality of instruction codes,

wherein operational clocks are inputted to the plurality of decode circuits and the plurality of execution circuits via the gated clock circuits, and

wherein the instruction location information decoder outputs control signals to stop the operation clock to the gated clock circuits corresponding to the fields ,where the NOP instructions are inserted before the plurality of instruction codes are compressed, on the basis of the instruction location information.

19. (Previously Presented) A semiconductor integrated circuit according to claim 18,

wherein the instruction unit further comprises a development buffer,

wherein the development buffer stores the plurality of instruction codes in the plurality of fields on the basis of the instruction location information, and

wherein the development buffer still stores preceding instruction codes in the fields, where the NOP instructions are inserted on basis of the instruction location information before the plurality of instruction codes are compressed, on the basis of the instruction location information.

20. (Previously Presented) The semiconductor integrated circuit according to claim 15, wherein the boundary area is an address range in which all bits are 0 or 1 the infra-page addresses.

21. (Previously Presented) The semiconductor integrated circuit according to claim 15,

wherein the boundary area is an address range in which all bits are 0 or 1 except for the lower n-bit of the infra-page addresses.

22. (Previously Presented) The semiconductor integrated circuit according to claim 15,

wherein the tag memory and the data memory comprises a memory cell, a sense amplifier and a precharge MOSFET,

wherein the sense amplifier amplifies and outputs a voltage outputted to a pair of bit lines from the memory cell,

wherein the bit lines are precharged via the precharged MOSFET, and

wherein the clocks switch the precharged MOSFET.

23. (Previously Presented) The semiconductor integrated circuit according to claim 15,

wherein the clock enable generating circuit comprises a first comparator, a second comparator, a register and a logical gate,

wherein the register stores the second logical page address,

wherein the first comparator compares the first logical page and the second logical page,

wherein the second comparator compares the whether a first intra-page address requested is not within the boundary addresses between intra-page addresses, and

wherein the logical gate generates a clock enable signal on the basis of outputs of the first comparator and the second comparator.